PVP 12

Code: EC7T5A

IV B.Tech - I Semester – Regular / Supplementary Examinations
November 2016

ADVANCED VLSI DESIGN
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Answer any FIVE questions. All questions carry equal marks

1. Predict and the evaluate the robustness of the CMOS inverter in Static behavior. 14 M

2. a) Memorize the advantages of BICMOS and GaAs devices. 6 M

   b) Design an inverter using BICMOS Logic and Explain. 8 M

3. a) Briefly Interpret the noise considerations in dynamic logic. 8 M

   b) Sketch the NAND gate using Pseudo static latch and explain. 6 M

4. Paraphrase the conceptual diagram of carry look ahead adder and also draw the schematic of mirror implementation of four bit look ahead adder. 14 M

5. Describe in detail about the booth multiplier with an example. 14 M

6. a) Criticize an 1 bit DRAM cell with its timing parameters and Explain. 7 M

b) Discuss about EPROM and EEPROM technologies in memories. 7 M

7. Summarize the functional and timing verification in design Verification. 14 M

8. Derive an SM chart for Binary multiplier and Explain. 14 M